ION-IMPLANTED K-BAND GaAs POWER FET

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ABSTRACT

This paper reports the performance up to 26 GHz from a GaAs power FET produced by ion implantation. At 15 GHz, an output power of 250 mW at 3 dB gain with 27.4% power-added efficiency was obtained. At 26 GHz, 55 mW at 3 dB gain with 5% power-added efficiency was demonstrated. Capless annealing and a novel lift-off gate fabrication scheme was employed.

Much progress has been made in the last few years in extending the frequency of operation and power handling capabilities of GaAs power field-effect transistors. This paper reports the performance results of a GaAs power FET capable of operation at frequencies as high as 26 GHz. At 15 GHz an output power of 250 mW at 3 dB gain was obtained with a maximum power-added efficiency of 27.4% from a 600 μm gate width cell. An output power of 160 mW at 3 dB gain and 14.5% power-added efficiency was realized at 20 GHz. The highest frequency result obtained was 55 mW with 3 dB gain and 5% power-added efficiency at 26 GHz. The active layers were formed by ion-implantation of ^{28}Si directly into a semi-insulating Cr-doped GaAs substrate. A novel lift-off gate fabrication process was developed to achieve a thick Ti/Pt/Au gate metallization with a submicrometer gate length.

The Si-implanted GaAs wafer was annealed under an arsenic overpressure using an operationally-simple capless annealing process[1]. The arsenic overpressure is maintained by a constant flow of AsH_3 and H_2 in an open quartz tube. The wafer was annealed at 825°C for 20 minutes. This annealing process produces a minimum spurious Cr redistribution effect on SI GaAs substrates implanted at the low fluence levels normally employed for FET fabrication. The SIMS profile in Figure 1 illustrates that only a

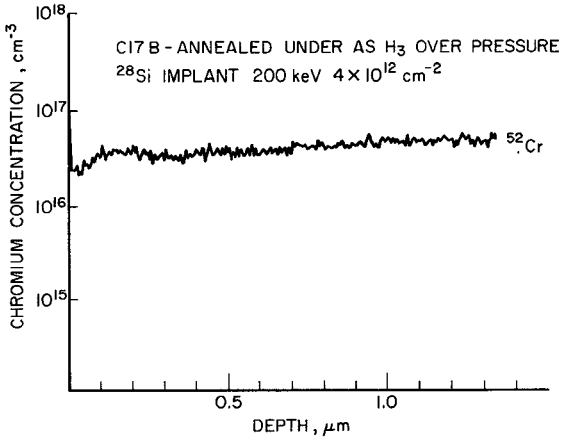

FIGURE 1. SIMS PROFILE FOR Cr AFTER CAPLESS ANNEALING.

slight depletion of Cr occurred at the surface in an Si-implanted ($4x10^{12}cm^{-2}$, 200 keV) capless annealed GaAs substrate. Strong Cr redistribution in SI GaAs has been reported for annealing with an Si_3N_4 encapsulant[2].

The electron density profile of the double-energy (50 keV and 180 keV) Si-implanted, capless-annealed wafer used for power FET fabrication is illustrated in Figure 2. The total fluence implanted

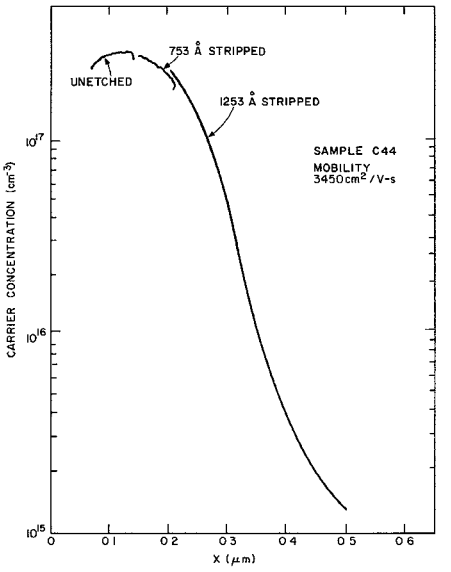

FIGURE 2. DOPANT DENSITY PROFILE.

was $6x10^{12}cm^{-2}$. The composite electron density profile was obtained from C-V measurement in combination with layer removal by chemical etching. The thickness of the chemically-removed layer was determined using a stylus depth meter (Tallysurf). The implant doses and energy were chosen to produce an active layer slightly thicker than that required for the finished device. This allowed a gate recess approximately 500Å deep to be produced. The gate recess aids in preventing premature source-to-drain burnout[3].

Device fabrication was standard except for the gate structure. Ohmic contacts were produced by lift-off of AuGe/Ni/Au and sintering at 450°C for 60 seconds in forming gas. Chemical etching of mesa structures was used for device isolation. The gate recess, nominally 1 μm long, was etched 1.5 μm away from the source electrode in a 4.5 μm ohmic contact separation. A two-layer photoresist technique similar to that developed by Dunkleberger[4] is employed to produce a photoresist mask with an undercut profile. The bottom photoresist layer acts as a spacer layer and helps to smooth out surface irregularities. The top photoresist layer is used

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to define a 1 μm gate opening by standard contact lithography. This photoresist structure is ideal for "lifting off" thick gate metallization. The device reported on here had an evaporated gate metallization consisting of 1000Å titanium, 1000Å platinum, and 12,000Å of gold. After lift-off, the titanium is chemically etched away[5] to reduce the effective gate length to submicrometer dimensions. Figure 3a shows a cross-section of a gate obtained in this manner. This gate structure allows a reduction in gate length without an accompanying increase in gate metal resistance. Very good control of the amount of undercut has been achieved. Figure 3b shows a typical section of the gate as viewed from underneath after etching away the GaAs substrate. Device fabrication is completed by electroplating thick gold on the sources, drain pad, and gate pad. The source posts are interconnected by flip-chip mounting to a gold-plated copper carrier for improved thermal resistance and low-source inductance[6].

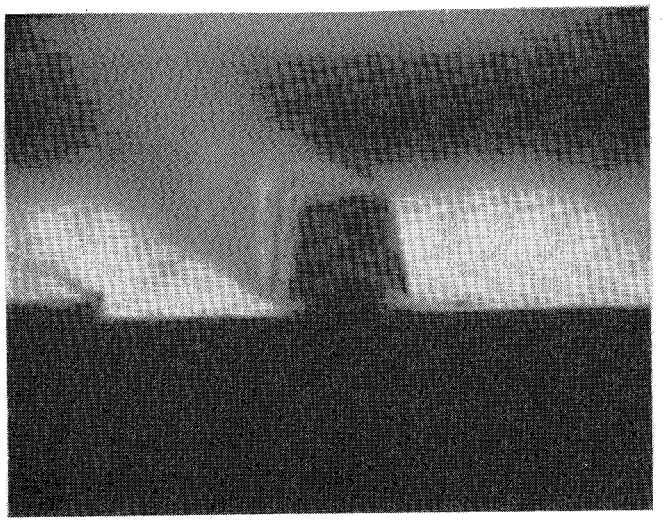

FIGURE 3a. CROSS SECTION OF CHEMICALLY-ETCHED GATE. MAGNIFICATION = 20,000X; GATE LENGTH ≃0.6 μm; TOTAL GATE METAL THICKNESS = 1.1 μm.

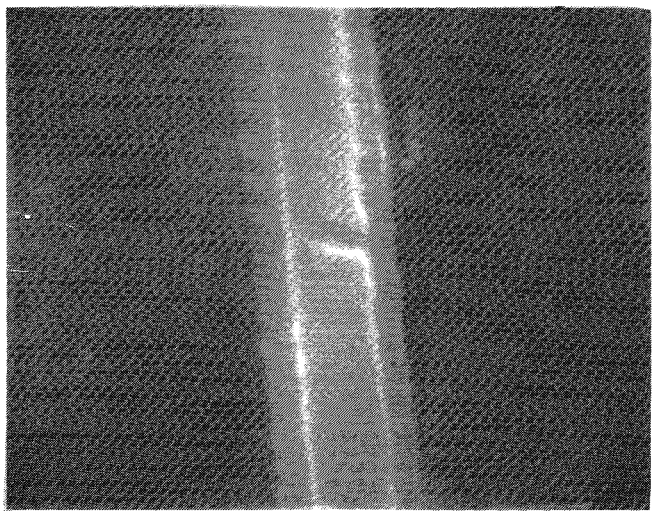

FIGURE 3b. VIEW OF UNDERSIDE OF CHEMICALLY-ETCHED GATE AFTER ETCHING AWAY THE GaAs SUBSTRATE. MAGNIFICATION = 20,000X.

The dc characteristics of a 150 μm wide section of the 600 μm unit cell device are shown in Figure 4. Figure 5 summarizes the output power obtained at 3 dB power gain and maximum power-added efficiency measured for a single 600 μm gate width cell as a function of frequency. The drain bias was 9 V during these measurements. At 15 GHz, an output power of 250 mW was obtained at 3 dB gain with a maximum power-added efficiency of 27.4%. The device demonstrated 160 mW with 3 dB gain and 14.5% power-added efficiency at 20 GHz. The highest frequency result obtained was 55 mW with 3 dB gain and 5% power-added efficiency at 26 GHz.

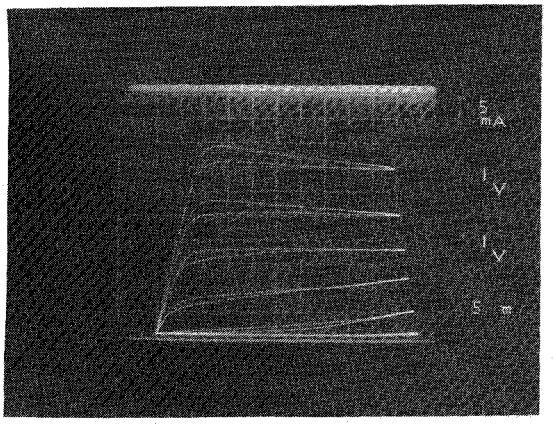

FIGURE 4. ELECTRICAL CHARACTERISTICS OF 150 μm WIDE SECTION OF 600 μm DEVICE CELL.
a) Current voltage characteristics of 150 μm wide section. Vertical scale = 5 mA/div.; Horizontal scale = 1 V/div.; Gate voltage = 1 V/step.

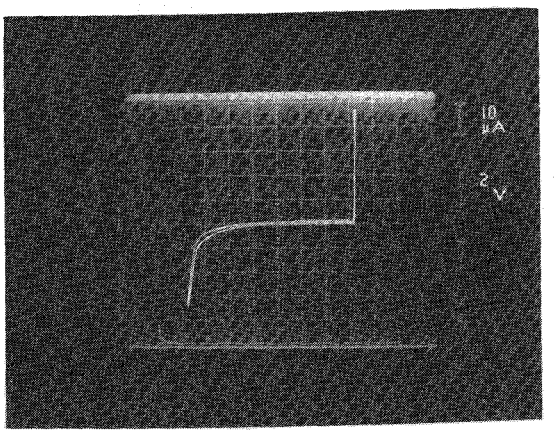

FIGURE 4. Same as above.
b) Gate-to-drain characteristics. Vertical scale = 10 μA/div.; Horizontal scale = 2 V/div.

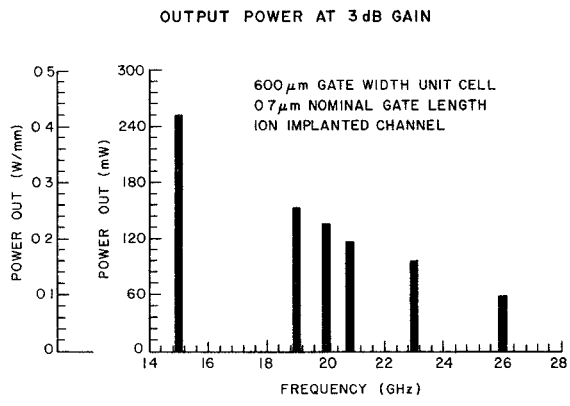

FIGURE 5a.

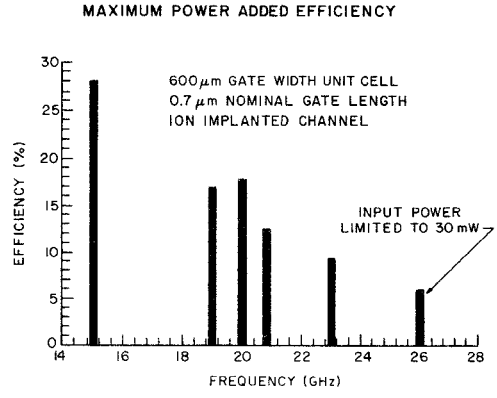

FIGURE 5b.

FIGURE 5. SATURATED POWER AND MAXIMUM EFFICIENCY OBTAINED FROM A 600 μm GATE WIDTH UNIT CELL. POWER OUTPUT PER UNIT GATE WIDTH IS SHOWN IN (a).

In summary we report power FET results up to 26 GHz. These results were achieved with a wafer produced using ion-implantation directly into an SI GaAs substrate and a capless-annealing process. A submicrometer gate length was produced using conventional contact photolithography by creating a "T" cross section gate by controlled lateral undercutting with a chemical etchant.

Acknowledgment

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